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(71) Applicant: Semiconductor Ideas to The Market
(ItoM) BV
4839 AH Breda (NL)

(72) Inventor: van Rumpt, Herman Wouter
5253 HC 'S-Hertogenbosch (NL)

(74) Representative: Van Straaten, Joop et al
Octrooibureau Van Straaten B.V.
Monseigneur Bosstraat 22
5401 EB Uden (NL)

(54) Receiver

(57) Receiver comprising a cascade of one to N resonance amplifiers (SA1, SA2, SA3), an output thereof being coupled to signal processing means for deriving a baseband modulation signal. To improve the signal to noise ratio said cascade is included in an RF input stage

of the receiver for a distributed selective amplification of an RF reception signal, preferably with an impedance level of the individual resonance amplifiers (SA1, SA2, SA3) within said cascade of first to N resonance amplifiers increasing in signal downstream direction.

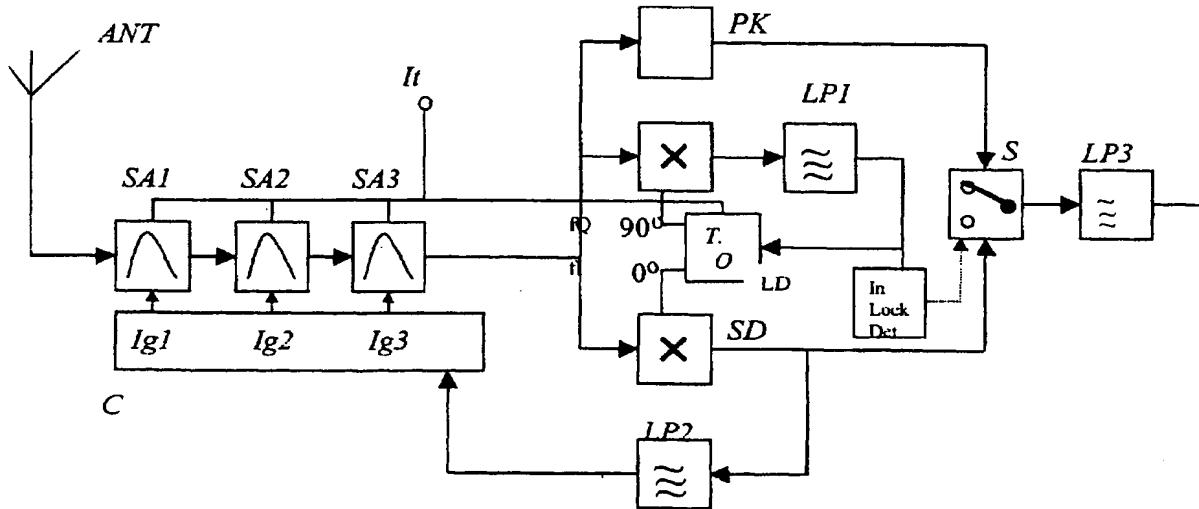


FIG 2

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Description

[0001] The invention relates to a receiver comprising a cascade of first to N resonance amplifiers, an output thereof being coupled to signal processing means for deriving a baseband modulation signal from a selected signal. Such receiver is known from US patent 5,220,686 and is based on a conventional superhet concept, in which said cascade is used in the IF part of the receiver to selectively amplify an IF signal.

[0002] Said cascade of first to N resonance amplifiers is on itself suitable for integration. However, the use thereof in a superhet receiver does not allow for full receiver integration, because of the specific system architecture of the conventional superhet concept. The advantages of fully integrated receiver architectures over conventional receiver architectures are known: they will offer a much smaller physical size and a much lower cost price. Such monolithically integrated receivers are in particular advantageous for use in specific applications, including clock controlled devices (e.g. radio's in PDAs, lap-tops, GSM, etc). Up to now the performance of these fully integrated receiver architectures was always lower due to the limitations of the signal processing properties of active devices compared to the (discrete) passive ones. Important indicators of signal processing performance are e.g. sensitivity, far-off and channel selectivity, dynamic range and tuning behaviour.

[0003] The cost price of a monolithic integrated receiver is, as of any IC, a complex quantity being determined a.o. by external components (X-tal, antenna, large time constants), chip area and yield (matching, spread).

[0004] It is a first object of the invention to offer a receiver architecture, which can be monolithically integrated.

[0005] It is a second object of the invention optimise the price/performance ratio of such monolithically integrated receiver.

[0006] It is a third object of the invention to provide measures to decrease the chip area of an integrated receiver without giving in on performance.

[0007] A receiver comprising a cascade of first to N resonance amplifiers, an output thereof being coupled to signal processing means for deriving a baseband modulation signal, according to the invention is therefore characterised in that said cascade is included in an RF input stage of the receiver for a distributed selective amplification of an RF reception signal.

[0008] The invention is based on the recognition that with a selective RF signal amplification distributed over a number of cascaded resonance amplifiers, various parameters of the individual resonance amplifiers, such as noise figure and far-off selectivity work out differently on the overall characteristic of the cascade, dependent on the position of the resonance amplifier in the cascade. The noise figure of the first resonance amplifier, i.e. the

resonance amplifier being first supplied with the RF reception signal, has a larger weight in the overall noise figure of the cascade as a whole than its succeeding or second resonance amplifier and so forth. On the other

5 hand, the far-off selectivity of the first resonance amplifier may be much less, or in other words the bandwidth may be larger, without giving in on the overall far-off selectivity of the cascade as a whole, than the second one, and so forth. With the measure according to the invention an optimised trade-off between said signal parameters can be obtained, allowing for further receiver signal processing with circuitry, which in itself is very much suitable for integration.

[0009] Therefore, a preferred embodiment of a receiver according to the invention is characterised in that the noise figure of the individual resonance amplifiers within said cascade of first to N resonance amplifiers decrease in signal upstream direction. For an implementation of this measure, use is made of the recognition that for a

10 selective resonance amplifier as mentioned above, $V_{noise} = \sqrt{fc/(B \cdot C)}$ in which V_{noise} represents the noise figure of a resonance amplifier, fc the center pass-band frequency of the resonance amplifier, B the bandwidth and C the capacitance value of the resonance amplifier and allows for an optimised trade off between V_{noise} , B and C per each resonance amplifier in the cascade, without affecting the overall noise figure of the cascade as a whole.

[0010] Preferably, a receiver according to the invention is characterised in that the impedance level of the individual resonance amplifiers within said cascade of first to N resonance amplifiers increase in signal downstream direction. This is equivalent to a decreasing scaling factor in downstream direction.

[0011] This measure according to the invention allows to decrease all set currents (I_g , I_t , I_{bw}) and also the capacitances C of the resonance amplifiers in the cascade in signal downstream direction, resulting in a decrease of the chip area needed. This reduction of scaling factor 20 per each resonance amplifiers in signal downstream direction substantially reduces the total needed chip area of the RF input circuit without affecting the performance compared with the known receiver with identical stages.

[0012] Another preferred embodiment of a receiver according to the invention optimised in terms of selectivity is characterised in that the bandwidth of the individual resonance amplifiers within said cascade of first to N resonance amplifiers decrease in signal downstream direction.

[0013] A further preferred embodiment of a receiver according to the invention is characterised in that the noise figure of the individual resonance amplifiers within said cascade of first to N resonance amplifiers decrease in signal upstream direction.

[0014] These and further aspects and advantages of the invention will be discussed more in detail hereinafter with reference to the disclosure of preferred embodiments, and in particular with reference to the appended

Figures, in which corresponding elements have like references, showing in:

Figure 1a a general circuitry diagram of a resonance amplifier for use in a receiver according to the invention;

Figure 1b-1d various modes of operation of the resonance amplifier of Figure 1a;

Figure 2 a first embodiment of a receiver according to the invention;

Figure 3 a second embodiment of a receiver according to the invention;

Figure 4 a signal plot showing the effect of a selectivity increase of the resonance amplifiers in downstream direction on the S/N ratio of the cascade as a whole;

Figure 5 a signal plot showing the effect of a scaling factor increase of the resonance amplifiers in downstream direction on the S/N ratio of the cascade as a whole.

[0015] Figure 1a shows a selective resonance amplifier SA corresponding to the one shown in Figure 3 of US patent nr 5 220 686. The resonance amplifier SA comprises a cascade of first and second controllable transconductance amplifiers TC1 and TC2, an output of TC2 being negatively fed back through an inverter INV to an input of TC1 and outputs of TC1 and TC2 being coupled to respective mass connected parallel RC members R1C1 and R2C2, TC1 and R1C1 respectively TC2 and R2C2 functioning as first and second active poly-phase transconductance filter sections. The common connections of TC1 and R1C1, respectively TC2 and R2C2, constitute quadrature current inputs I_{in}, respectively I'_{in} and/or quadrature voltage outputs V_{out}, respectively V'_{out}. A set current I_t can be supplied to control terminals of TC1 and TC2 to set the transconductance of TC1 and TC2 and therewith the resonance frequency f_{res} of the resonance amplifier SA to a predetermined value. The resonance amplifier SA is also provided with third and fourth controllable transconductance amplifiers TC3 and TC4, each of which is fed back from the output to the input and is arranged at the outputs of TC1 and TC2, respectively. These transconductance amplifiers TC3 and TC4 realise an extra negative resistor, which can be considered to be arranged parallel to the parallel RC members R1C1 and R2C2, respectively. By applying a fixed set current I_{bw} to control terminals of TC3 and TC4, the transconductance of TC3 and TC4 and therewith the bandwidth or selectivity of the resonance amplifier SA can be set to a predetermined value without affecting its tuning frequency. Fifth and sixth transconductance amplifiers TC5 and TC6 are included between quadrature voltage inputs V_{in} and V'_{in} of the resonance amplifier SA on the one hand and the above current inputs I_{in} and I'_{in} of the resonance amplifier SA on the other hand. By supplying a gain control current I_g to control terminals of TC5 and TC6 the overall

gain of the resonance amplifier SA can be varied without affecting the resonance frequency f_{res} and/or the bandwidth of the resonance amplifier SA. In the embodiment shown, the resonance amplifier SA can be used to selectively amplify a pair of phase-quadrature signals, hereinafter referred to as first amplification mode.

[0016] By mutually coupling the quadrature voltage inputs V_{in} and V'_{in}, respectively the quadrature voltage outputs V_{out} and V'_{out}, as shown in Figure 1b, the resonance amplifier SA can be used to selectively amplify a single phase input signal into a single phase output signal hereinafter referred to as second amplification mode.

[0017] By mutually coupling the quadrature voltage inputs V_{in} and V'_{in} of the resonance amplifier SA, as shown in Figure 1c, the resonance amplifier SA selectively amplifies a single phase input signal, while converting the same into a pair of phase-quadrature output signals V_{out} and V'_{out}, this mode of operation of the resonance amplifier SA being hereinafter referred to as third amplification mode.

[0018] By mutually coupling the quadrature voltage outputs V_{out} and V'_{out}, the resonance amplifier SA selectively amplifies a pair of phase-quadrature input signals while converting the same into a mon-phase output signal, this mode of operation of the resonance amplifier being hereinafter referred to as fourth amplification mode.

[0019] The description of the resonance amplifier SA given so far is sufficient for a proper understanding of the invention. For more information of the resonance amplifier SA, reference is made to the above US patent 5 220 686.

[0020] Figure 2 shows an embodiment of a receiver according to the invention comprising a cascade of respectively first to N (N=3) resonance amplifiers SA1, SA2, SA3, hereinafter also referred to as "cascade", for a selective amplification of an RF reception signal being supplied from antenna means ANT to an RF input of the cascade. Each of the resonance amplifiers SA1, SA2, SA3 correspond to the one of Figure 1b operating in the above second amplification mode, however according to the invention, they differ mutually in their settings with regard to the bandwidth or selectivity and/or their scaling factor or impedance level, such that:

- the bandwidth of SA3 is smaller than the bandwidth of SA2 and the bandwidth of SA2 is smaller than the bandwidth of SA1, i.e. the bandwidth of the resonance amplifiers SA1, SA2 and SA3 decreases in signal downstream direction. Such bandwidth setting is obtained by a proper set value for the bandwidth set currents I_{bw} of SA1, SA2 and SA3. The selectivity of the resonance amplifiers SA1, SA2 and SA3 therewith increases in signal downstream direction.
- the bias setpoints or scaling factor of the resonance amplifier SA1 is larger than the bias setpoints or

scaling factor of the resonance amplifier SA2, which in its turn is larger than the bias setpoints or scaling factor of the resonance amplifier SA3. As a result thereof the capacitance C and therewith the impedance level of SA1, SA2 and SA3 increases in signal downstream direction allowing to reduce the chip area, necessary for an implementation of the cascade, without giving in on the overall noise figure of the cascade.

Said cascade of first to N resonance amplifiers is coupled to baseband signal demodulation means comprising a.o. a tuning oscillator TO providing a pair of phase quadrature oscillator signals $f_i(0^\circ)$ and $f_q(90^\circ)$, the in-phase oscillator signal $f_i(0^\circ)$ being supplied as a local synchronous RF carrier to a carrier input of the synchronous detector SD and the quadrature phase oscillator signal $f_q(90^\circ)$ being provided to a carrier input of the phase detector PD. The tuning oscillator TO is preferably implemented by using a regeneratively feedback resonance amplifier (not shown). The phase detector PD is included in a phase locked loop (PLL) comprising a loop filter LP1 coupled between an output of PD and a tuning control input of the tuning oscillator TO. The PLL provides a negative feedback of phase differences between the carrier signal of the selectively amplified output signal of the cascade on the one hand and the phase quadrature oscillator signal of TO on the other hand, therewith phase synchronising the pair of phase quadrature oscillator signals to the incoming RF carrier signal. The tuning oscillator TO is also manually variable to a wanted RF carrier frequency with a tuning control current I_t supplied to a tuning control input of the tuning oscillator TO. Along with the tuning of TO, the tuning control current I_t is also supplied to tuning inputs of SA1, SA2 and SA3 to secure a mutually parallel tuning between TO on the one hand and SA1, SA2 and SA3 on the other hand. Outputs of the synchronous detector SD and the amplitude detector PK are coupled to first and second switching terminals of a switching device S for connecting one of those detectors to a common output terminal of the switching device S. Said common switching device output terminal is coupled to baseband modulation signal processing means, comprising a lowpass filter LP3 for selecting the useful baseband modulation signal, e.g. an audiosignal, from the output signal of the switching device S.

[0021] The switching device S is controlled by an in-lock detector LD being coupled between an output of the loop filter LP1 on the one hand and a switching control terminal of the switching device S on the other hand and detecting the in-lock state of the PLL from the level of the oscillator phase control signal in the PLL. The implementation of such in-lock detector LD lies within the normal abilities of the skilled man, reason for which no further details of the in-lock detector LD is given. The in-lock detector LD controls the switching device S to couple an output of the synchronous detector SD to the

common output terminal of the switching device S when the PLL is locked to a wanted RF carrier frequency and to couple the amplitude detector PK to said common output terminal when the PLL is out of lock. If in lock,

- 5 the output signal of SD provides a better signal-to-noise ratio than the output signal of PK. If the PLL is out of lock, i.e. $f_i(0^\circ)$ is not phase/frequency synchronised with the RF carrier signal at the output of the cascade, then it is the amplitude detector PK providing a better signal-to-noise ratio than the synchronous detector SD. This secures an optimal reception of the receiver in terms of signal to noise ratio at varying signal reception quality.
- 10 [0022] The gain distribution of the resonance amplifiers SA1, SA2 and SA3 is chosen to optimise for the noise figure of the cascade as a whole. Preferably, the signal gain per each resonance amplifier SA1, SA2 and SA3 is chosen to decrease in signal downstream direction. Furthermore, the receiver shown is provided with an AGC loop, which includes the synchronous detector SD being coupled through a lowpass filter LP2 to an input of gain control signal generating means C. The gain control signal generating means C derives gain control currents I_g1 , I_g2 and I_g3 from the output signal of the lowpass filter LP2 being supplied to gain control input terminals of the respective resonance amplifiers SA1, SA2 and SA3 of the cascade, such that any deviation in the signal input level of SD (and therewith also any deviation in the signal input level of PD and PK) from a predetermined set level is negatively fed back to the gain control input terminals of the respective resonance amplifiers SA1, SA2 and SA3. This results in a reduction of such deviations, therewith effecting a stabilisation of said signal input level at said predetermined set level.
- 15 [0023] Preferably, the gain factors of the gain control currents I_g1 , I_g2 and I_g3 in the AGC loop are chosen to mutually deviate, such that a variation of the RF input signal level causes the gain of the first resonance amplifier SA1 to vary stronger than the gain of the second resonance amplifier SA2 and the gain of the second resonance amplifier SA2 to vary stronger than the gain of the third resonance amplifier SA3 of the cascade. This measure results in a further improvement of the signal-to-noise ratio of the cascade, which come in addition to the improvement in signal-to-noise ratio obtained with the above settings of SA1, SA2 and SA3.
- 20 [0024] The gain control ranges of SA1, SA2 and SA3 are furthermore chosen to be mutually shifted to provide a deferred or delayed amplification in the respective resonance amplifiers at a decrease of the received RF signal carrier. Such deferred or delayed amplification is as such known and is to maximise the overall range of linear amplification of the cascade.
- 25 [0025] The implementation of gain control signal generating means C providing the above specified functions lies on itself within the ability of one skilled in the art.
- 30 [0026] The AM-receiver shown in this Figure 2 is suitable for monolithic integration and may be used for receiving various different categories of broadcasting sig-

nals, such as e.g. radio broadcast AM-signals, vestigial sideband television broadcast signals, etc..

[0027] Figure 3 shows a second embodiment of a receiver according to the invention in which the first resonance amplifier SA1 in the cascade operates in the above third mode of amplification, i.e. the inputs being coupled in accordance with the resonance amplifier SA as shown in Figure 1c, and in which the second and third resonance amplifier SA2 and SA3 both operate in the above first mode of operation. The antenna means ANT supply a single phase RF input signal to the input of the first resonance amplifier SA1, in which it is selectively amplified and phase splitted in a pair of phase quadrature signals being supplied to a pair of phase quadrature input terminals of the second resonance amplifier SA2. In SA2 a further selective amplification takes place, the quadrature relationship of the pair of phase quadrature signals being further improved by the suppression of non-orthogonal frequency components occurring in the I and Q parts of the filter sections of the resonance amplifier SA2. The pair of phase quadrature signals is again selectively amplified and improved in its quadrature phase relationship the third resonance amplifier SA3.

[0028] SA3 supplies the in-phase component I of the so amplified pair of phase quadrature signals to a signal input of the synchronous detector SD, and the phase quadrature component Q thereof to a signal input of the phase detector PD. The phase detector PD is included in a PLL, which further includes a first lowpass filter LP1, in the loop being followed by a lowpass filter LP4, which provide a tuning control signal to the tuning oscillator TO. The tuning oscillator TO generates a pair of phase quadrature signals $f_i(0^\circ)$ and $f_q(90^\circ)$, the in-phase oscillator signal $f_i(0^\circ)$ being supplied to a carrier input of the synchronous detector SD, the phase quadrature oscillator signal $f_q(90^\circ)$ being supplied to a carrier input of phase detector PD. The PLL of this receiver functions in accordance with the PLL of the receiver of Figure 2, in that it provides a negative feedback of phase differences between the carrier signal of the selectively amplified output signal of the cascade on the one hand and the phase quadrature oscillator signal of TO on the other hand, therewith phase synchronising the pair of phase quadrature oscillator signals to the incoming RF carrier signal.

Unlike the receiver of Figure 2, the use of an amplitude detector, an in-lock detector and a switching device is avoided in the present receiver in that an output of the synchronous detector SD is followed through a lowpass filter LP5 by a first squaring device SQ1 and an output of the first lowpass filter LP1 by a second squaring device SQ2. Outputs of these first and second squaring devices SQ1 and SQ2 are coupled to an adder device AD providing an signal addition of the squared components I^2 and Q^2 of the phase quadrature baseband amplitude modulation signal of the RF input signal, resulting in a detection of said baseband amplitude modulation signal being reflected in $v(I^2 + Q^2)$. Although not

strictly necessary, this baseband amplitude modulation signal may optionally be further selected in a lowpass filter LP6 following the adder device AD.

[0029] The output of the adder device AD is fed back to the cascade through a second lowpass filter LP2, therewith forming an AGC loop, functioning in accordance with the AGC described with reference to the receiver of Figure 2.

[0030] Also this second embodiment of the receiver according to the invention is suitable for monolithic integration, while providing at least comparable receiver performance as non-integratable receivers such as those using the above superhet receiver concept.

[0031] Figure 4 shows a signal plot demonstrating the increase in signal to noise ratio or noise figure as a function of the RF signal voltage input level for an existing prior art Philips IC TEA 5551 in curve a, for an existing prior art Philips IC TEA 5762 in curve b, for a cascade with SA1, SA2 and SA3 having mutually equal bandwidth or selectivity $Q=5$ in curve c and for a cascade with SA1, SA2 and SA3 having increasing bandwidth or selectivity Q in signal downstream direction according to the invention: for SA1: $Q1=2$; for SA2: $Q2=5,5$ and for SA3: $Q3=10$ in curve d. The scaling factors or impedance levels of the resonance amplifiers SA1, SA2 and SA3 in all these cases have been chosen at a mutually equal value 1.

The improvement in signal-to-noise ratio (or sensitivity) resulting from the increase in bandwidth or selectivity in signal downstream direction appears clearly for RF signal voltage input levels below 50 dBuV.

[0032] Figure 5 shows a signal plot demonstrating the increase in signal to noise ratio as a function of the RF signal voltage input level for the above existing prior art Philips IC TEA 5551 in curve a, for the above existing prior art Philips IC TEA 5762 in curve b, for a cascade with SA1, SA2 and SA3 having respective bandwidth or selectivity values $Q1=2$; $Q2=5$ and $Q3=10$ in signal downstream direction according to the invention and

mutually equal scaling factor or impedance value 1 in curve c and for a cascade with SA1, SA2 and SA3 having respectively the same increasing bandwidth or selectivity values $Q1=2$; $Q2=5,5$ and $Q3=10$ as well as respective scaling factors or impedance levels $SF1=2$, $SF2=0,75$ and $SF3=0,25$ according to the invention in curve d. The improvement in signal to noise ratio obtained with the measure to decrease the scaling factor or to increase the impedance level for the resonance amplifiers SA1, SA2 and SA3 in the cascade in signal downstream direction comes in addition to the improvement resulting from the increase in bandwidth of the resonance amplifiers SA1, SA2 and SA3 in the cascade in signal downstream direction, as becomes most clearly apparent for RF signal voltage input levels below 42 dBuV.

[0033] The person skilled in the art of radio design will recognize further policies to be followed within the ambit of the present invention, the scope of which has justfully

been determined by the appended claims hereinafter. For example, the invention can be used not only in AM radio and AM vestigial sideband television signals, but in all types of receivers, using a selective RF part. Furthermore, the cascade may include any number of resonance amplifiers, the AGC circuit may be simplified to control the gain of the resonance amplifiers in the cascade similarly. The fixed setting of the bandwidth of the resonance amplifiers SA1, SA2 and SA3 in accordance with the invention may be realised electronically by applying a properly chosen fixed set current Ibw to TC3 and TC4 of the respective resonance amplifiers SA1, SA2 and SA3, as described above. However, the noise figure of the resonance amplifiers SA1, SA2 and SA3 may be further be reduced by leaving out TC3 and TC4 and by dimensioning R1C1 and R2C2 in each such resonance amplifier, such that a bandwidth setting of the resonance amplifiers SA1, SA2 and SA3 is obtained, which is in accordance with the above chosen selectivities of SA1, SA2 and SA3 according to the invention. Apart from the reduction of the noise figure, this also reduces the circuit lay out complexity and the necessary chip area of each resonance amplifier.

Claims

6. Receiver according to one of claims 1 or 5, characterised by control means included in a gain control loop for controlling the gain of said cascade of N resonance amplifiers to provide a gain control signal amplification for the respective first to N resonance amplifiers in the cascade, which decreases in signal downstream direction.
7. Receiver according to one of claims 1 to 6 comprising a tuning oscillator, **characterised in that** the tuning oscillator provides a pair of I and Q oscillator signals, the I signal being supplied to a synchronous detector and the Q oscillator signal being provided to a phase detector included in a phase locked loop, an output of the synchronous detector being coupled to a first switching terminal of a controllable switching device, said phase locked loop being coupled to an in-lock detector supplying a switching control signal to a switching control terminal of said controllable switching device for switching through the output signal of the synchronous detector to baseband modulation signal processing means when the phase locked loop is in phase lock with an RF input carrier signal.
8. Receiver according to claim 7, **characterised in that** the output of the cascade of first to N resonance amplifiers is followed by an amplitude detector, having an output being coupled to a second switching terminal of the controllable switching device for switching through the output signal of the amplitude detector to said baseband modulation signal processing means when the phase locked loop is out of lock.
9. Receiver according to one of claims 1 to 6, characterised by the cascade of first to N resonance amplifiers providing a pair of phase quadrature signals, the in-phase component thereof being supplied to a synchronous detector, the quadrature phase component thereof being supplied to a phase detector included in a phase locked loop, outputs of the synchronous detector and the phase detector being selectively respectively coupled to first and second squaring devices, outputs of said squaring devices being coupled to signal inputs of an adder circuit having an output followed by baseband modulation processing means.
10. Receiver according to claim 9, **characterised in that** an output of the adder device is included in an AGC loop controlling the gain factor of each of the first to N resonance amplifiers in the cascade.
11. Receiver according to one of claims 1 to 10, characterised by said resonance amplifiers comprising active poly-phase transconductance filter sections.

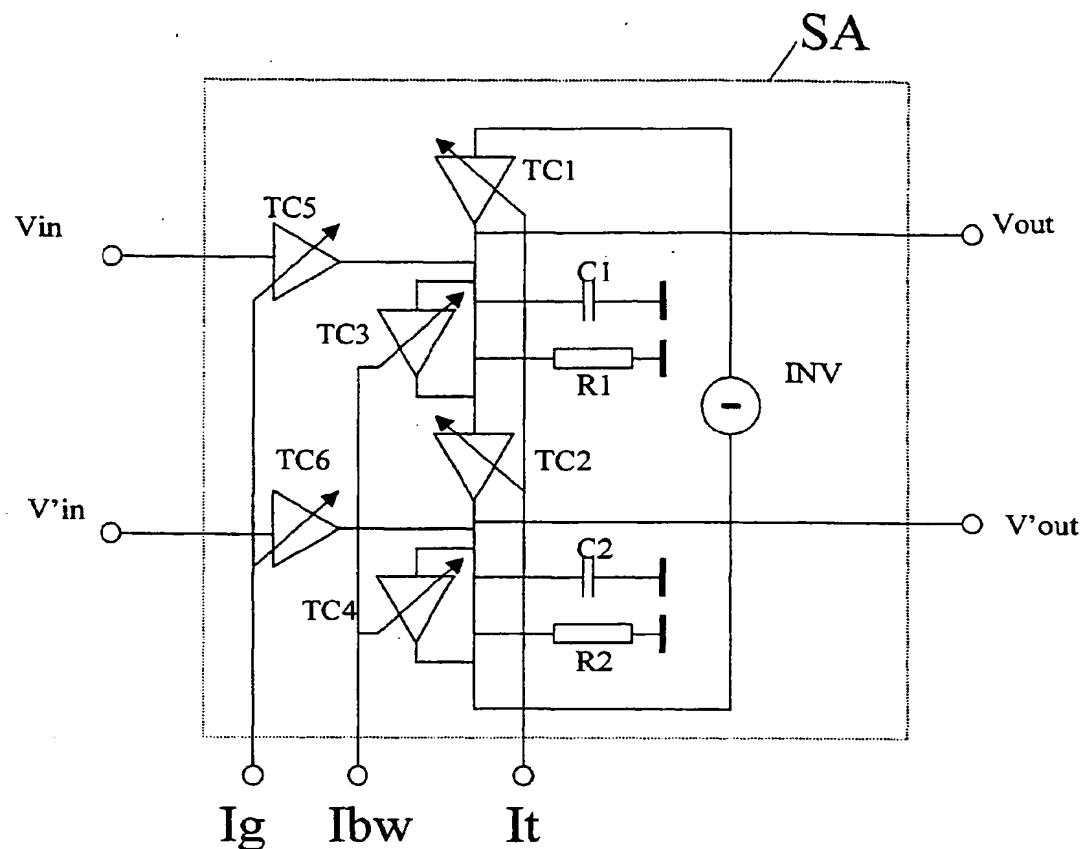


FIG 1a

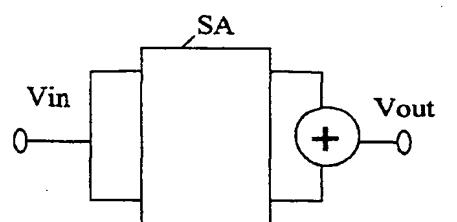


Fig 1b

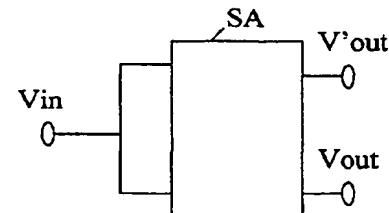


Fig 1c

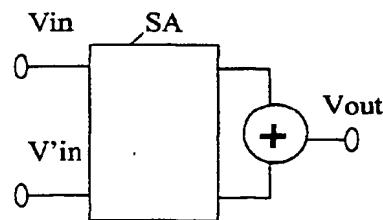


Fig 1d

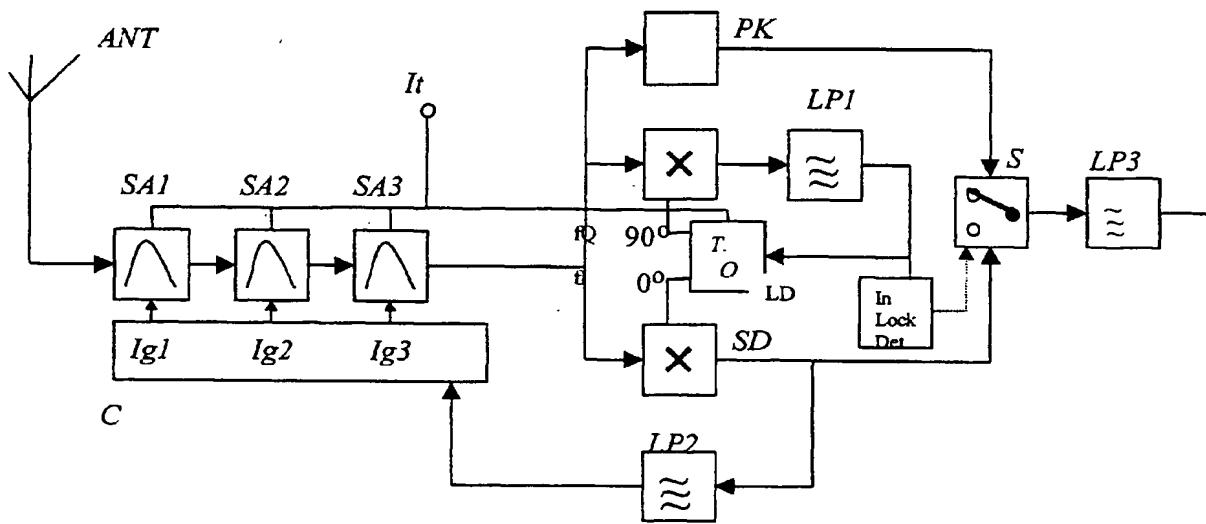


FIG 2

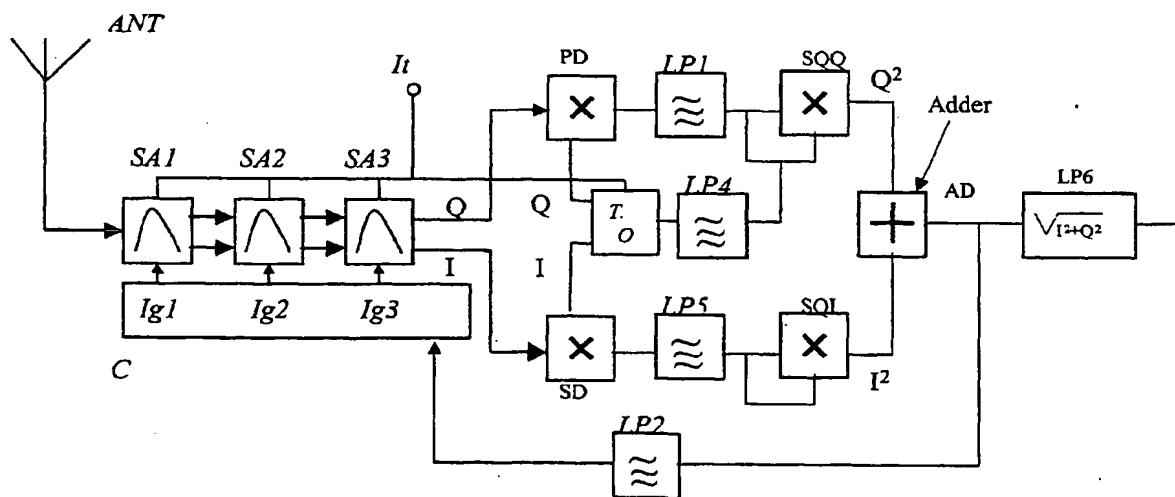
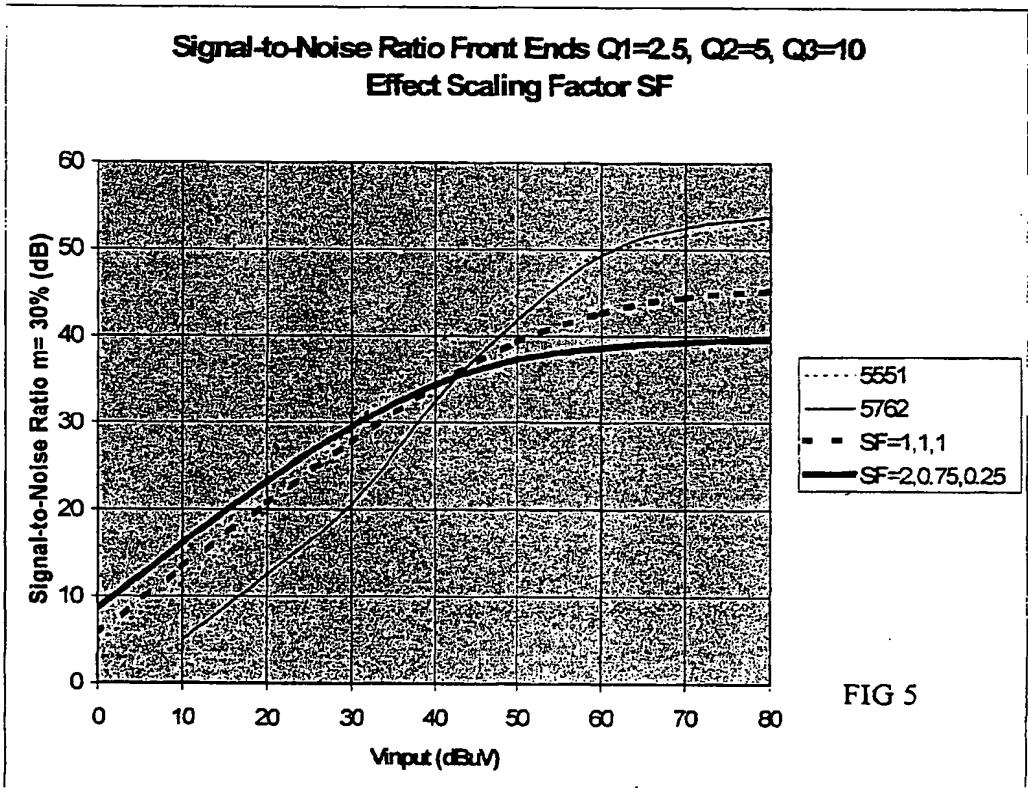
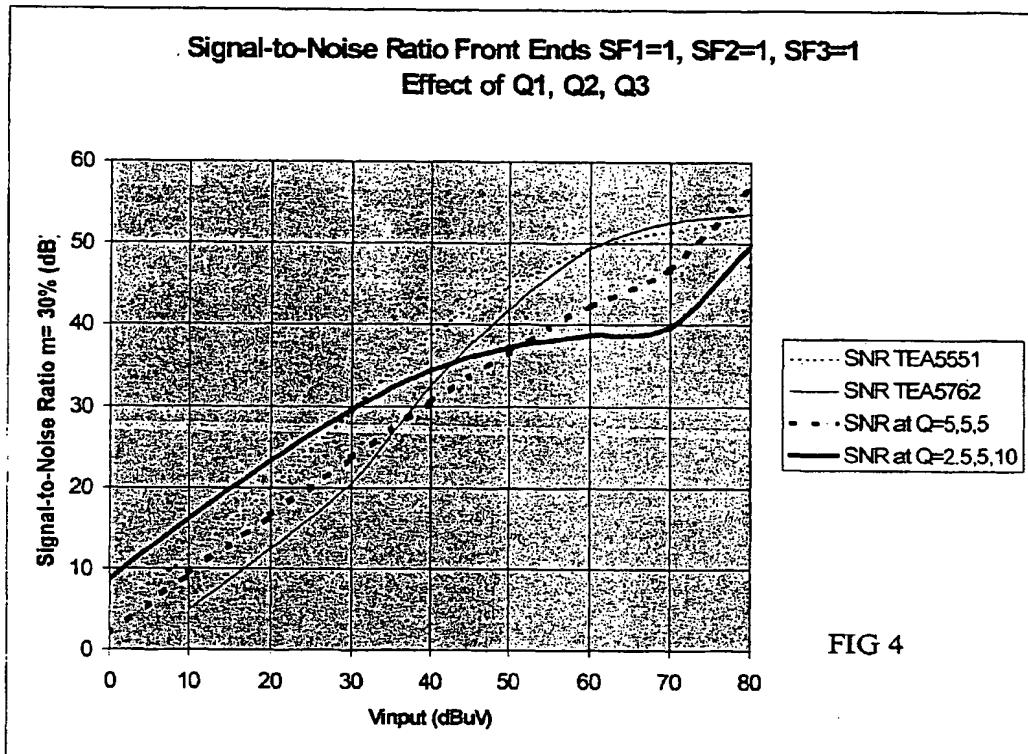


FIG 3





European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 00 20 0644

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (IntCl.7)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
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A	TOYODA I ET AL: "THREE-DIMENSIONAL MASTERSLICE MMIC ON SI SUBSTRATE" IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, US, IEEE INC. NEW YORK, vol. 45, no. 12, PART 02, 1 December 1997 (1997-12-01), pages 2524-2530, XP000732041 ISSN: 0018-9480 * figure 12A *	1	
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<p>The present search report has been drawn up for all claims</p>			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	25 July 2000	Peeters, M	
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**ANNEX TO THE EUROPEAN SEARCH REPORT
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